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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/537,666	06/06/2005	Chris Wyland	US02 0512 US	6346

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EXAMINER

ARORA, AJAY

ART UNIT PAPER NUMBER

2811

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/537,666

Applicant(s)

WYLAND ET AL.

Examiner

Ajay K. Arora

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 6/6/05 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 6/6/05.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## **DETAILED ACTION**

### ***Information Disclosure Statement***

The information disclosure statement filed 6/6/2005 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

### ***Specification***

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

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The use of the trademark TEFLON® and KAPTON® has been noted in this application.

It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

The abstract of the disclosure is objected to because the submitted abstract includes information other than the abstract. Correction is required. See MPEP § 608.01(b).

The disclosure is objected to because of the following informalities:

On page 1, line 30, it is not clear what the word "them" refers to; i.e. does it refer to bond wires, the strip line or the ground planes.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 5 and 6 rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "the upper strip line and the lower strip line are glued together,

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sealing a space accommodating the plurality of bond wires", does not reasonably provide enablement for "hermetically sealing". The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims. Hermetic sealing implies extreme air tightness and it is not clear how it may be achieved with the structure and materials disclosed in the specification.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Cheng (US 6,707,164), hereinafter Chen.

Regarding Claim 1, Chen (refer to Figure 7) teaches an integrated circuit device (IC), having signal connections, power connections, and ground connections (Col. 5, lines 27-35), the integrated circuit having been placed in a package substrate (12), the package substrate having signal pad connections, power connections, and ground connections (Col. 5, lines 27-35), a method for building a structure having interconnect

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wire bonds having controlled impedance, the method comprising: bonding a lower strip line (21a) coupling a first ground connection (21) of the IC to a first package substrate ground (Col. 6, lines 1-7) connection (30); bonding with a plurality of wires (23a), a plurality of signal pads (23) on a device die, coupling the plurality of signal pads to signal pad connections (60) on the package substrate, the plurality of signal pads in proximity to the first ground connection and the plurality of wires maintained at a first predetermined distance from the lower strip line (21a); and bonding an upper strip line (24a) coupling a second ground connection of the IC with a second package substrate ground connection, the upper strip line maintained at a second predetermined distance from the plurality of wires. Note that since no dimensions or construction have been defined for a strip line, the bond wires discussed above may also be referred to as "strip lines".

Regarding Claim 4, Chen (refer to Figure 7) teaches strip line structure controlling impedance of bond wires in an integrated circuit device (IC) placed in a package, the strip line structure comprising: a lower strip line (21a), coupling a first ground connection (21) in the IC with a first ground (Col. 6, lines 1-7) connection (30) in the package; an upper strip line, coupling a second ground connection on the IC with a second ground connection in the package, the lower strip line and upper strip line (24a) being a predetermined distance apart from one another, forming a space accommodating a plurality of bond wires (23a) whose wire diameters are less than the predetermined distance, the bond wires not in electrical contact with the upper strip line and the lower

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strip line (Col. 6, lines 1-7), the bond wires coupling a signal pin on the IC with a signal connection in the package .

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2, 3 and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng in view of Lamson (US 6,822,340), hereinafter Lamson.

Regarding Claim 2, Cheng (refer to Figure 7) teaches the claimed methods including the upper strip line (24a) and the lower strip line (21a) but fails to teach sealing openings (of the said conductors) with a dielectric material, thereby trapping air in the structure. Lamson teaches a wirebonded semiconductor package wherein the openings (i.e. open surface of the conductors) are sealed with a dielectric material, thereby trapping air in the structure (Col. 2, lines 45-48). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Cheng so that the method includes sealing openings in the upper strip line and the lower strip line with a dielectric material, thereby trapping air in the structure. The ordinary artisan

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would have been motivated to modify Cheng for at least the purpose of providing a low dielectric constant medium surrounding the above conductors (Col. 2, lines 45-48).

Regarding Claim 3, Lamson teaches that the dielectric material is a glue (Col. 4, lines 64-67). Note that any material that acts as an adhesive may be considered as glue.

Regarding Claim 5, Cheng teaches substantially the claimed structure but does not teach that the upper strip line and the lower strip line are “glued together, hermetically sealing a space accommodating the plurality of bond wires”. Lamson teaches (refer to Figure 4b) a wirebonded semiconductor device wherein multiple conductors (wirebonds) that are “glued together, sealing a space accommodating the plurality of bond wires” (Col. 4, lines 48-56, note that the molding compound can be considered a glue since it acts as an adhesive). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Cheng so that the upper strip line and the lower strip line are glued together, sealing a space accommodating the plurality of bond wires. The ordinary artisan would have been motivated to modify Cheng for at least the purpose of providing a specific dielectric constant medium surrounding the above conductors.

Regarding Claim 6, Cheng teaches substantially the claimed structure but does not teach that the space contains a dielectric selected from at least one of the following: vacuum, partial vacuum, nitrogen, oxygen, argon, xenon, neon, aerogels, and foams.



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Lamson teaches (refer to Figure 4b) a wirebonded semiconductor device wherein the space contains oxygen (since air is trapped in the foamed polymer coating the conductors, see Col. 2, lines 45-48). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Cheng so that the space contains a dielectric selected from at least one of the following: vacuum, partial vacuum, nitrogen, oxygen, argon, xenon, neon, aerogels, and foams. The ordinary artisan would have been motivated to modify Cheng for at least the purpose of using a material capable of providing a low dielectric constant (Col. 4, lines 57-60).

Regarding Claim 7, Cheng (refer to Figure 7) teaches substantially the claimed structure including the strip line structure wherein the upper strip line (24a) and lower strip line (21a) are in proximity with the plurality of bond wires (23a). However, Cheng fails to teach that the said conductors (24a and 21a) have "an insulating material deposited on a side". Lamson teaches a wirebonded semiconductor package wherein conductors have an insulating material deposited on a side (Col. 2, lines 45-48). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Cheng so that the said conductors have "an insulating material deposited on a side". The ordinary artisan would have been motivated to modify Cheng for at least the purpose of preventing shorting between the minute, closely spaced conductors (Col. 1, lines 50-53).

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Regarding Claim 8, Cheng teaches substantially the claimed structure but does not teach that insulating material is selected from at least one of the claimed materials including polyimide. Lamson teaches a wirebonded semiconductor package wherein the insulating material is polyimide (Col. 2, lines 55-58). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Cheng so that the insulating material is polyimide. The ordinary artisan would have been motivated to modify Cheng for at least the purpose of using a material capable of forming a foamed polymer dielectric coating (Col. 4, lines 57-60), which achieves a low dielectric constant.

Regarding Claim 9, Cheng teaches substantially the claimed structure but does not teach that the plurality of bond wires are "covered with an insulating coating" selected from at least one of the claimed materials, including polyimide. Lamson teaches a wirebonded semiconductor package wherein the bond wires are covered with an insulating coating (Col. 2, lines 45-48) and the insulating material is polyimide (Col. 2, lines 55-58). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Cheng so that the plurality of bond wires are "covered with an insulating coating" selected from at least one of the claimed materials, including polyimide. The ordinary artisan would have been motivated to modify Cheng for at least the purpose of using a material capable of forming a foamed polymer dielectric coating (Col. 4, lines 57-60), which achieves a low dielectric constant.

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Claims 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng in view of Grellman (US 4,600,907), hereinafter Grellman.

Regarding Claim 10, Cheng teaches substantially the claimed structure but does not teach that the upper strip line and the lower strip line are comprised of copper. Grellman teaches an semiconductor package wherein the interconnect connector (microstraps 28, 30 and 32 in Figure 1) may be comprised of copper (Col. 4, lines 57-60). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Cheng so that the upper strip line and the lower strip line are comprised of copper. The ordinary artisan would have been motivated to modify Cheng for at least the purpose of using a high conductivity material (Col. 4, lines 48-50) that is also malleable to form thin conductors.

Regarding Claim 11, Cheng teaches substantially the claimed structure but does not teach that the upper strip line and the lower strip line are comprised of gold. Grellman teaches an semiconductor package wherein the interconnect connector (microstraps 28, 30 and 32 in Figure 1) may be comprised of gold (Col. 4, lines 57-60). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Cheng so that the upper strip line and the lower strip line are comprised of gold. The ordinary artisan would have been motivated to modify Cheng for at least the purpose of using a high conductivity material (Col. 4, lines 48-50) that has minimal degradation in conductivity over time.

Regarding Claim 12, Cheng teaches substantially the claimed structure but does not teach that the upper strip line and the lower strip line are comprised of silver. Grellman teaches an semiconductor package wherein the interconnect connector (microstraps 28, 30 and 32 in Figure 1) may be comprised of silver (Col. 4, lines 57-60). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Cheng so that the upper strip line and the lower strip line are comprised of silver. The ordinary artisan would have been motivated to modify Cheng for at least the purpose of using a high conductivity material (Col. 4, lines 48-50) that is cheaper than gold.

Regarding Claim 13, Cheng teaches substantially the claimed structure but does not teach that the upper strip line and the lower strip line are comprised of aluminum. Grellman teaches an semiconductor package wherein the interconnect connector (microstraps 28, 30 and 32 in Figure 1) may be comprised of aluminum (Col. 4, lines 57-60). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Cheng so that the upper strip line and the lower strip line are comprised of aluminum. The ordinary artisan would have been motivated to modify Cheng for at least the purpose of using a high conductivity material (Col. 4, lines 48-50) that is lighter and not expensive.

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Regarding Claim 14, Cheng teaches substantially the claimed structure but does not teach that the upper strip line and the lower strip line are comprised of a highly conductive material selected from: copper, gold, silver, aluminum and an alloy thereof. Grellman teaches an semiconductor package wherein the interconnect connector (microstraps 28, 30 and 32 in Figure 1) may be comprised of a highly conductive material selected from: copper, gold, silver, aluminum and an alloy thereof (Col. 4, lines 57-60). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Cheng so that the upper strip line and the lower strip line are comprised of a highly conductive material selected from: copper, gold, silver, aluminum and an alloy thereof. The ordinary artisan would have been motivated to modify Cheng for at least the purpose of using a high conductivity material (Col. 4, lines 48-50) that has limited deterioration with time and is malleable enough for forming thin conductors.

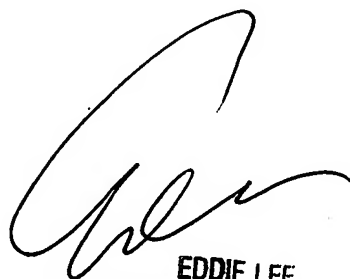
### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ajay K. Arora whose telephone number is (571) 272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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